REMARKS

Entry of this Amendment if proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 1-26 are all the claims presently pending in the application. Claims 1-6 and 9-13 stand rejected on prior art grounds. Applicant gratefully acknowledges that claims 16-26 are allowed and respectfully requests that these claims be passed to issue. Applicant further acknowledges that claims 7, 8, 14, and 15 would be allowable if rewritten in independent form. This Amendment amends claims 1 and 9. Attached hereto is a marked up version of the changes made in the claims by the current Amendment.

The claims are amended to merely clarify the subject matter of the claims and in not to narrow the scope of the claims in order to overcome the prior art or for any statutory purposes of patentability. Notwithstanding any claim amendments of the present Amendment or those amendments that may be made during prosecution, Applicant's intent is to encompass equivalents of all claim elements. Reconsideration in view of the foregoing amendments and the following remarks is respectfully solicited.

Applicant respectfully traverses the Examiner's objection under 35 U.S.C. § 132 for alleged new matter in claim 1. The added material is clearly supported by the original disclosure. For example, on page 17, lines 5-10 of the specification, an exemplary embodiment of the claimed invention is described where "the PNP transistors Tr_0 and Tr_{n+1} are physically arranged at positions shown in Figure 5," (emphasis Applicant's). Referring to Figure 5 of the Application, the final stage of the exemplary first current mirror circuit is transistor Tr_{n+1}, which is clearly located at a point farthest away from the reference current input terminal Tr_0 than any of the other transistors in the first current mirror circuit.

Further, the specification recites that transistor Tr_0 (e.g., the reference current input terminal) is "physically arranged at the closest position to the power supply terminal 11," and that transistor Tr_{n+1} (e.g., the final stage of the first current mirror circuit) is "physically arranged at the farthest position from the power supply terminal 11," (Application, p. 17, lines 5-10). Therefore, transistor Tr_{n+1} must be arranged at a position farthest from transistor Tr_0.

However, Applicant has deleted this element from claim 1 because it is not necessary for patentability of the invention.

Regarding the prior art rejections, claims 1-3, 6, 9, 10, and 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Emeigh et al (Emeigh) (U.S. Patent No. 5,767,698), claims 4 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Emeigh in view of Nayebi (U.S. Patent No. 6,384,638), and claims 5 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Emeigh in view of Nayebi and further in view of Kipnis (U.S. Patent No. 6,326,836).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention, as disclosed and claimed, for example by independent claim 1, is directed to a driving circuit (and a constant current driving apparatus using the driving circuit), which includes a first current mirror circuit which outputs a plurality of output currents each of which corresponds to a reference current, a reference current input terminal for supplying the reference current to the first current mirror circuit, and a second current mirror circuit which converts a polarity of an output current outputted from a final stage of the first current mirror circuit and outputs the converted output current.

The conventional driving circuit has a current mirror circuit to drive a load at a constant current. This circuit employs the method of independently setting an input current of the current mirror circuit by adjusting the resistive value. Thus, it is difficult to reduce variation in the reference currents of driving circuits when a plurality of driving circuits are used to drive, such as an LED panel, a device at a constant current.

The claimed device, on the other hand, includes a driving circuit that has a first current mirror circuit which outputs a plurality of output currents which correspond to a reference current. A value of the reference current corresponds to the value of an output from a final stage of the first mirror circuit and to a value of an output from a second current mirror circuit (Application, p. 16, lines 4-12).

Providing output currents that correspond to a reference current is important because when there are irregular components in output currents outputted from the output terminals of driving circuits in a display panel, the irregularities cause a variation to be induced in a light emission amount of the light emission device. As a result, a display irregularity is generated in the display panel (Application, p.3, lines 20-27).

However, in the present invention, values of output currents of a driving circuit correspond to a value of a reference current to the driving circuit, thereby providing additional driving circuits with output currents corresponding to the original reference current and consistent output currents to a light emission device.

II. THE PRIOR ART REJECTIONS

THE EMEIGH REFERENCE

Regarding the 35 U.S.C. § 102(e) rejection to claims 1-3, 6, 9, 10, and 13, the

Examiner alleges Figures 4 and 5 of Emeigh teach a driving circuit as described in claim 1, which includes "a first current mirror circuit" 32, 32', which "outputs a plurality of output currents" at the drain terminals of transistors T1-T3, T1'-T3', "each of which corresponds to a reference circuit" (e.g., reference current IREF from circuit 20).

Applicant respectfully submits the Examiner is incorrect. Emeigh fails to teach or suggest "a plurality of output currents each of which corresponds to a reference current," as recited in claim 1. The output currents of T1, T2, and T3 (and T1'-T3') in Emeigh do not "correspond" to reference current signal IREF, and therefore Emeigh cannot anticipate, or for that matter render obvious, claim 1.

As is clear from Emeigh's disclosure referring to Figure 4, transistors T1-T3 have varying width to length ratios as compared to transistor T0, thereby scaling the reference current (Figure 5 and corresponding reference numerals to those in Figure 4 are incorporated herein by reference). The result is current output values from transistors T1-T3 that are many times higher than the value of the reference current IREF in Emeigh's disclosure. "Transistor T3 preferably has a width to length ratio (W/L) that is three times that of transistor T0, thereby scaling the reference current signal by a factor of three at its first terminal," (col. 7, lines 33-36) (emphasis Applicant's). Moreover, "[t]he W/L's of transistors T1 and T2 are preferably about five times that of transistor T0, thus scaling the reference current signal by a factor of five," (Emeigh, col. 7, lines 56-58) (emphasis Applicant's). There is absolutely no disclosure or suggestion that first stage current mirror 32 outputs a plurality of output currents, each of which corresponds to a reference current, as in independent claim 1.

Therefore, there is no teaching or suggestion in Emeigh of "a first current mirror circuit which outputs a plurality of output currents each of which corresponds to a reference

current," as recited in claim 1 (emphasis Applicant's). As discussed above, this feature is important because when there are irregular components in output currents outputted from the output terminals of driving circuits in a display panel, the irregularities cause a variation to be induced in a light emission amount of the light emission device. As a result, a display irregularity is generated in the display panel (Application, p.3, lines 20-27).

Indeed, "correspond" is defined in Webster's Dictionary as "to be in agreement or conformity, match, to be similar or analogous.[1] The outputs of transistors T1-T3 in Emeigh are scaled up at three to five times the current of the reference current IREF and therefore do not "correspond" to the reference current, in the context of the claimed invention.

Outputting a higher and/or varying current from first current mirror circuit outputs (as in Emeigh) in the present invention would be detrimental to the claimed driving circuit. Outputting irregular currents in output terminals that do not correspond to a reference current is a problem with conventional devices that is solved by the present invention (see Application, p. 3, line 3 to p. 6, line 20).

Further, the Examiner alleges that second stage current mirror 34 in Figure 4 (34' in Figure 5) of Emeigh converts a polarity of an output current at the drain terminal of transistor T3 or drain terminal of transistor T3'. However, the only current conversion described for transistor T3 regarding Figures 4 and 5 is that transistor T3 scales the reference currents signal by a factor of three (Emeigh, col. 7, lines 30-35). There is no disclosure or suggestion that a second current mirror circuit in Emeigh converts a polarity of an output current from a final stage of the first current mirror circuit. Therefore, Emeigh cannot anticipate or render obvious

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[1]See attached page 183, Webster's Universal College Dictionary, 1997 ed., pub. Gramercy Books, NY (1997).

the claimed combination including "a second current mirror circuit which converts a polarity of an output current outputted from a final stage of said first current mirror circuit and outputs the converted output current," as recited in claim 1.

Thus, turning to the exemplary language of claim 1, there is no teaching or suggestion of "*[a] driving circuit comprising:*

a first current mirror circuit which outputs a plurality of output currents each of which corresponds to a reference current;

a reference current input terminal for supplying said reference current to said first current mirror circuit; and

a second current mirror circuit which converts a polarity of an output current outputted from a final stage of said first current mirror circuit and outputs the converted output current, (emphasis Applicant's).

Thus, claims 1-3, 6, 9, 10, and 13 are patentable over Emeigh.

THE NAYEBI REFERENCE

Regarding the rejections to claims 4 and 11, the Examiner alleges the claims are obvious as being unpatentable over Emeigh in view of Nayebi. Applicant submits that Nayebi would not have been combined with Emeigh, absent hindsight. Nayebi discloses a differential charge pump for providing a low charge pump current. Nayebi is a different technology for a different aim than Emeigh, and furthermore does not even disclose a current mirror circuit. Therefore, there is certainly no motivation to combine a reference for a differential charge pump with a reference for a current mirror circuit, absent hindsight.

Further, even if the references were combined, the combination would not have taught

or suggested the claimed invention.

The deficiencies of Emeigh have been discussed above, and Nayebi fails to make up for these deficiencies. Specifically, Nayebi does not teach or suggest a current mirror circuit, or for that matter a current mirror circuit with a plurality of outputs that correspond to a reference current. Therefore, there is no teaching or suggestion that Nayebi's method and materials for manufacturing circuits for a differential charge pump renders obvious the claimed invention.

Therefore, claims 4 and 11 are patentable over Emeigh in view of Nayebi.

THE KIPNIS REFERENCE

The Examiner rejected claims 5 and 12 as being unpatentable over Emeigh in view of Nayebi, and in further view of Kipnis. Applicant submits that Kipnis would not have been combined with Emeigh and Nayebi, absent hindsight. The structure of Kipnis is different from that of Emeigh, Nayebi, and even the present invention. Kipnis does not teach or suggest a current mirror circuit with a plurality of outputs. Further, neither Emeigh, Nayebi, nor Kipnis teach or suggest output currents that correspond to a reference current. Therefore, there is no motivation to combine with Emeigh and Nayebi to provide "a base current compensation circuit for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit," as cited by the Examiner, since this is not the purpose of the base current compensation circuits of the claimed invention.

Indeed, the base current compensation circuits of the claimed invention are for the purpose of providing each circuit an output current that corresponds to the reference current for the first mirror circuit (see Application, p. 23, lines 1-25). There is no motivation to

combine Kipnis with Emeigh and Nayebi since the claimed invention would neither be taught nor suggested by the combination.

Further, even if the references were combined, the combination would not have taught or suggested the claimed invention. The deficiencies of Emeigh have been discussed above, and Kipnis fails to make up for these deficiencies. Specifically, Kipnis discloses an input current being gain divided to form a current smaller than the input current by a magnitude of the gain. The gain divided current being transferred through an intermediate current mirror with optional gain and to provide an output current (Abstract).

However, Kipnis does not teach or suggest a current mirror circuit with a plurality of outputs that correspond to a reference current. An input current in Kipnis is "gain divided to form a current smaller than the input current," as described above. Therefore, Kipnis cannot make up for the deficiencies of Emeigh and Nayebi, and claims 5and 12 are patentable over the urged combination of references.

For the reasons stated above, the claimed invention is fully patentable over the cited references and the Examiner is respectfully requested to withdraw the rejections.

IV. INFORMAL MATTERS AND CONCLUSION

Claim 9 has been amended to overcome the Examiner's objection.

Claim 1 has been amended, and therefore overcomes the Examiner's objection.

In view of the foregoing, Applicant submits that claims 1-26, all the claims presently either rejected or objected to in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to withdraw the rejections and pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner may contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 5/22/03

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Amendment by facsimile with the United States Patent and Trademark Office to Examiner Long T. Nguyen, Group Art Unit 2816 at fax number (703) 872-9319 this 22nd day of May, 2003.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1 and 9 have been amended, as follows:

1. (Twice Amended) A driving circuit comprising:

a first current mirror circuit which outputs a plurality of output currents each of which corresponds to a reference current;

a reference current input terminal for supplying said reference current to said first current mirror circuit; and

a second current mirror circuit which converts a polarity of an output current outputted from a final stage of said first current mirror circuit and outputs the converted output current[,].

[wherein said final stage of said first current mirror circuit is arranged in a position farthest away from said reference current input terminal.]

9. (Amended) The driving circuit according to claim 1, wherein said first current mirror circuit [comprising] further comprises:

[a reference current input terminal to which said reference current is supplied;]

a ground terminal which is connected to a ground;

a first circuit provided between said reference current input terminal and said ground terminal, to determine said plurality of output currents;

a common ground line which extends from said ground terminal;

a plurality of output terminals;

a plurality of second circuits provided between said common ground line and said plurality of output terminals, to output a part of said plurality of output currents determined by said first circuit through said plurality of output terminals; and

a third circuit provided at a next stage of said plurality of second circuits as said final stage of said first current mirror circuit, to output said output current determined by said first circuit.